

Appl. No. 09/751,427
Am dt. dated February 10, 2004
Reply to Office Action of December 10, 2003

REMARKS

This Amendment is in response to the Office Action mailed December 10, 2003. In the Office Action, the Examiner rejected claims 1-6, 8-12, 14-17, 19-23, and 25 under 35 U.S.C. § 102, and rejected claims 7, 13, 18, and 24 under 35 U.S.C. § 103. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102

2. The Examiner rejects claims 1-6, 8-12, 14-17, 19-23, and 25 under 35 U.S.C. § 102(e) as being anticipated by Arends et al. (US 6,560,712).

As per claims 1 and 14, the Examiner asserts that Arends discloses each and every limitation of the claims citing column 4, lines 17-61. Arends discloses an apparatus in which a processor can be activated to respond to an arbitration signal and generate a bus grant signal to an alternate bus master without requiring the processor to exit the low power mode. Col. 4, line 35, through col. 5, line 30. Applicant respectfully submits that the apparatus of Arends does not disclose the present invention which provides that a peripheral device becomes the default bus master when a processor that is the default bus master enters a low power mode. A default bus master retains control of the bus except for those times when the default bus master grants control to an alternate bus master. Specification page 6, line 22, through page 7, line 14. Thus the processor disclosed by Arends remains the default bus master even when in the low power mode. Applicant has amended claims 1 and 14 to make clear that a peripheral device becomes the default bus master when the processor enters a second power management state. The use of two different devices as default bus masters is distinctly different from the apparatus of Arends which has a single default bus master that can handle bus arbitration while remaining in the low power state.

As per claim 2, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

As per claims 3 and 16, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional limitations recited. Applicant has amended claims 3 and 16 to be consistent with the claim amendments in claims 1 and 14.

As per claims 4, 15, and 20, the Examiner asserts that Arends discloses a first peripheral device communicatively coupled to the configurable link wherein the second level of access the peripheral device is capable of operating as the default bus master for the computer without assistance from the CPU, citing column 3, line 28, through column 4, line 61. The Examiner states that "bus arbitration in low power system provide arbitration of system bus independent of operating state of the processor." Applicant respectfully submits that the ability of the processor to serve as the default bus master while remaining in a low power mode does not disclose an apparatus that causes another device to operate as the default bus master without assistance from the processor when the processor is in a low power mode as

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claimed. Applicant has amended claims 4, 15, and 20 to be consistent with the claim amendments in claims 1 and 14.

As per claims 5 and 19, the Examiner asserts that Arends discloses a peripheral device coupled to the configurable link causes the configurable link to operate in the second level of access when the CPU is in a second power management state, citing column 3, line 28, through column 4, line 61. Applicant respectfully submits that nothing in Arends discloses the configurable link operating in a second level of access wherein the processor is not the default bus master. Applicant has amended claims 5 and 19 to be consistent with the claim amendments in claims 1 and 14.

As per claim 6 and 17, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional limitations recited.

As per claim 8, the Examiner asserts that Arends discloses the transfer rate over the configurable link in the second level of access is different than in the first level of access, citing column 4, lines 38-41. The cited portion of Arends discloses shutting off clock signals to shut down the processor and the system in low power mode. Applicant does not understand shutting down the clock signals as disclosed to disclose a transfer rate that varies based on two levels of access as claimed. Rather, Figure 5 suggests that the clock rate for transfers on SYS BUS are the same regardless of whether the processor is running (clocks C1 and C2 active) or in low power mode (clocks C1 and C2 stopped). Applicant has amended claim 8 to be consistent with the claim amendments in claim 1.

As per claim 9, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited. Applicant has amended claim 9 to be consistent with the claim amendments in claim 1.

As per claim 10, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited. Applicant has amended claim 10 to be consistent with the claim amendments in claim 1.

As per claim 11, the Examiner asserts that Arends discloses the configurable link enables the first peripheral device to manage the input/output hub to control communications to and from the first peripheral device in the second level of access, citing column 2, lines 50-63, and column 3, line 28-column 4, line 38. Arends does not disclose an input/output hub. Further, Arends discloses an apparatus in which the processor always controls the communications even when in a low power state. Arends cannot disclose a configurable link enables a first peripheral device to manage an input/output hub to control communications to and from the first peripheral device in a second level of access as claimed. Applicant has amended claim 11 to be consistent with the claim amendments in claim 1.

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As per claim 12, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

As per claim 21, the Examiner asserts that Arends discloses each and every claimed limitation including a sub-system to configure a link coupling the input/output hub to a first peripheral device to allow the first peripheral device to manage data flow over the hub if the central processor is in a second power management state, citing column 3, line 28-column 4, line 38. Arends discloses an apparatus in which a processor can be activated to respond to an arbitration signal and generate a bus grant signal to an alternate bus master without requiring the processor to exit the low power mode. Col. 4, line 35, through col. 5, line 30. Applicant respectfully submits that the apparatus of Arends does not disclose the present invention which provides that a sub-system couples a peripheral device as the default bus master when a processor that is the default bus master enters a low power mode. A default bus master retains control of the bus except for those times when the default bus master grants control to an alternate bus master. Specification page 6, line 22, through page 7, line 14. Thus the processor disclosed by Arends remains the default bus master even when in the low power mode. Applicant has amended claim 21 to make clear that a peripheral device becomes the default bus master when the processor enters a second power management state. The use of two different devices as default bus masters is distinctly different from the apparatus of Arends which has a single default bus master that can handle bus arbitration while remaining in the low power state.

As per claim 22, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

As per claim 23, the Examiner asserts that Arends discloses a sub-system to buffer data at the first peripheral device if the central processor is in the second power management state, citing column 3, line 28-column 4, line 38. The Examiner does not present any support for this assertion beyond the citation. Applicant is unable to find any disclosure of buffering data at the first peripheral device if the central processor is in the second power management state as claimed.

As per claim 25, the Examiner asserts that Arends discloses a sub-system to delay the central processor from transitioning from the second power management state to the first power management state, citing column 4, lines 35-61. The Examiner does not present any support for this assertion beyond the citation. Applicant is unable to find any disclosure of delaying the central processor from transitioning from the second power management state to the first power management state as claimed.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-6, 8-12, 14-17, 19-23, and 25 under 35 U.S.C. § 102(e) as being anticipated by Arends.

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Rejection Under 35 U.S.C. § 103

4. The Examiner rejects claims 7 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Arends et al. (US 6,560,712) in view of Odaohhara (US 6,574,740).

Applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional limitations recited.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 7 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Arends in view of Odaohhara.

5. The Examiner rejects claims 13 and 24 under 35 U.S.C. § 103(a) as being unpatentable over Arends et al. (US 6,560,712) in view of Hannah (US 5,784,581).

Applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional limitations recited.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 13 and 24 under 35 U.S.C. § 103(a) as being unpatentable over Arends in view of Hannah.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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